What is claimed is:

1. A method to control a switchable decoupling capacitor in an integrated circuit device comprising:

providing an integrated circuit device comprising a switchable decoupling capacitor;

initializing said switchable decoupling capacitor by a method comprising:

connecting said switchable decoupling capacitor between a power supply and ground; and

storing the state of said switchable decoupling capacitor as enabled;

thereafter controlling said switchable decoupling capacitor during operation of said integrated circuit device by a method comprising:

monitoring a voltage on a terminal of said switchable decoupling capacitor;

disconnecting said switchable decoupling capacitor if said voltage exceeds a threshold level; and

storing said state of said switchable decoupling capacitor as disabled if said switchable decoupling capacitor is disconnected.

2. The method according to Claim 1 wherein said switchable

decoupling capacitor comprises a capacitor and a switch connected in series.

3. The method according to Claim 2 wherein said capacitor comprises a PMOS gate, wherein a first terminal of said capacitor is connected to said power supply, wherein a second terminal of said capacitor is connected to a first terminal of said switch, and wherein a second terminal of said switch is connected to said ground.

4. The method according to Claim 2 wherein said switch comprises a CMOS transfer gate.

5. The method according to Claim 2 wherein said capacitor comprises a NMOS gate, wherein a first terminal of said capacitor is connected to said ground, wherein a second terminal of said capacitor is connected to a first terminal of said switch, and wherein a second terminal of said switch is connected to said power supply.

6. The method according to Claim 1 wherein said step of monitoring a voltage across said switchable decoupling capacitor comprises coupling said voltage to the input of an inverter.

7. The method according to Claim 6 further comprising disabling said inverter when said voltage exceeds said threshold level.

8. The method according to Claim 1 wherein said step of storing the state of said switchable decoupling capacitor as enabled and said step of storing the state of said switchable decoupling capacitor as disabled are performed by a latch.

9. The method according to Claim 1 wherein said steps of connecting and disconnecting said switchable decoupling capacitor comprises generating a signal and wherein said signal is used to control additional said switchable decoupling capacitors.

10. A method to control a switchable decoupling capacitor in an integrated circuit device comprising:

providing an integrated circuit device comprising a switchable decoupling capacitor wherein said switchable decoupling capacitor comprises a capacitor and a switch connected in series;

initializing said switchable decoupling capacitor by a

method comprising:

connecting said switchable decoupling capacitor between a power supply and ground; and

storing the state of said switchable decoupling capacitor as enabled;

thereafter controlling said switchable decoupling capacitor during operation of said integrated circuit device by a method comprising:

monitoring a voltage on a terminal of said switchable decoupling capacitor by coupling said voltage to the input of an inverter;

disconnecting said switchable decoupling capacitor if said voltage causes said inverter to switch; and

storing said state of said switchable decoupling capacitor as disabled if said switchable decoupling capacitor is disconnected.

11. The method according to Claim 10 wherein said capacitor comprises a PMOS gate, wherein a first terminal of said capacitor is connected to said power supply, wherein a second terminal of said capacitor is connected to a first terminal of said switch, and wherein a second terminal of said switch is connected to said ground.

12. The method according to Claim 10 wherein said switch comprises a CMOS transfer gate.

13. The method according to Claim 10 wherein said capacitor comprises a NMOS gate, wherein a first terminal of said capacitor is connected to said ground, wherein a second terminal of said capacitor is connected to a first terminal of said switch, and wherein a second terminal of said switch is connected to said power supply.

14. The method according to Claim 10 further comprising disabling said inverter when said voltage causes said inverter to switch.

15. The method according to Claim 10 wherein said step of storing the state of said switchable decoupling capacitor as enabled and said step of storing the state of said switchable decoupling capacitor as disabled are performed by a latch.

16. The method according to Claim 10 wherein said steps of

connecting and disconnecting said switchable decoupling capacitor comprises generating a signal and wherein said signal is used to control additional said switchable decoupling capacitors.

17. An integrated circuit device comprising:

a switchable decoupling capacitor coupled between a power supply and ground capacitor wherein said switchable decoupling capacitor comprises a capacitor and a switch connected in series;

a means to initialize said switchable decoupling capacitor;

a means to monitor a voltage on a terminal of said switchable decoupling capacitor;

a means to control said switch based on said voltage; and

a means to store the state of said switchable decoupling capacitor.

18. The device according to Claim 17 wherein said capacitor comprises a PMOS gate, wherein a first terminal of said capacitor is connected to said power supply, wherein a second terminal of said capacitor is connected to

a first terminal of said switch, and wherein a second terminal of said switch is connected to said ground.

19. The device according to Claim 17 wherein said switch comprises a CMOS transfer gate.

20. The device according to Claim 17 wherein said capacitor comprises a NMOS gate, wherein a first terminal of said capacitor is connected to said ground, wherein a second terminal of said capacitor is connected to a first terminal of said switch, and wherein a second terminal of said switch is connected to said power supply.

21. The device according to Claim 17 wherein said means to monitor a voltage on a terminal of said switchable decoupling capacitor comprises an inverter.

22. The device according to Claim 21 wherein said inverter further comprises a means to disable said inverter when said voltage causes said inverter to switch.

23. The device according to Claim 17 wherein said means to store the state of said switchable decoupling capacitor comprises a latch.

24. The device according to Claim 23 wherein said means to initialize said switchable decoupling capacitor comprises a second switch to turn ON said switchable decoupling capacitor switch during initialization.

25 The device according to Claim 17 wherein said means to control said switchable decoupling capacitor comprises a signal and wherein said signal is used to control additional said switchable decoupling capacitors.